REMARKS

The Office Action dated November 20, 2003, has been received and reviewed.

Claims 31-35 and 37-45 are currently pending and under consideration in the above-referenced application, each standing rejected.

Claims 32-35 and 37-45 have been amended to replace each occurrence of the term "said" with "the." As these are equivalent terms, none of these revisions narrows the scope of any of claims 32-35 or 37-45.

Reconsideration of the above-referenced application is respectfully requested.

Rejections Under 35 U.S.C. § 112, First Paragraph

Claims 37-41, 44, and 45 stand rejected under 35 U.S.C. § 112, first paragraph, for purportedly containing subject matter which was not adequately described in the specification.

Specifically, the Office has asserted that the as-file specification does not provide support for "providing a HSG polysilicon layer on [a] storage poly structure and lining . . . recesses with a dielectric material . . ." Office Action dated November 20, 2004, pages 2 and 3.

Please note that the claims of the above-referenced application are not method claims. As such, none of the claims of the above-referenced application is drawn to "providing a HSG polysilicon layer." Instead, some of the claims recite structures which include a hemispherical-grain polysilicon layer.

First, it is respectfully submitted that the as-filed specification of the above-referenced application provides adequate written support for the hemispherical-grain polysilicon layer of claims 37-41, 44, and 45

Although the specification of the above-referenced application does not expressly describe that remaining portions of an HSG polysilicon layer are removed from a storage poly structure prior to the formation of a capacitor dielectric layer thereover, it is respectfully submitted that leaving the HSG polysilicon in place would not be an affirmative act. As such, it is respectfully submitted that one of ordinary skill in the art would readily recognize from the

disclosure of the above-referenced application that any remaining portions of the HSG polysilicon layer may remain in place prior to forming a dielectric layer over the exposed surfaces of the storage poly structure.

Moreover, one of ordinary skill in the art would readily understand that it does not matter if any remaining HSG polysilicon remained in place on the storage poly structure, as the HSG polysilicon may have substantially the same electrical conductivity properties as the remaining portions of the underlying polysilicon layer. This is one of the reasons why, following the patterning of the underlying polysilicon layer, the HSG polysilicon does not appear as a separate element. To many of skill in the art, the extra process steps that would be required to remove the HSG polysilicon and clean the structure would be undesirable, as extra process steps increase the likelihood of damage to a device under fabrication and, thus, the probability of device failure.

Since one of ordinary skill in the art would readily recognize that remaining HSG polysilicon may be either left on or removed from the storage poly structure, it is respectfully submitted that the as-filed specification of the above-referenced application provides an adequate written description of the subject matter recited in claims 37-41, 44, and 45.

Second, it is respectfully submitted that the as-filed specification of the above-referenced application provides adequate written support for the recitation of "dielectric material at least lining . . . recesses" in claims 37-41, 44, and 45.

In this regard, FIG. 10 illustrates a capacitor structure in which recesses, or "openings 134" (page 8, lines 21-23), are lined with a "dielectric material layer 138" (page 8, lines 23-26). In addition, page 11, line 28, to page 12, line 3, of the as-filed specification describes "depositing a dielectric material layer over [an] etched structure 152..."

It is, therefore, respectfully submitted that the as-filed specification of the above-referenced application provides an adequate written description of the subject matter recited in claims 37-41, 44, and 45.

For these reasons, it is respectfully submitted that each of claims 37-41, 44, and 45 is in compliance with the requirements of the first paragraph of 35 U.S.C. § 112. Therefore,

withdrawal of the 35 U.S.C. § 112, first paragraph, rejections of claims 37-41, 44, and 45 is respectfully requested.

Rejections Under 35 U.S.C. § 112, Second Paragraph

Claims 31-35 and 40 stand rejected under 35 U.S.C. § 112, second paragraph, for assertedly being indefinite.

In particular, it has been asserted that the terms "contiguous mesas" and "contiguous webs" are indefinite.

The third edition of the American Heritage College Dictionary defines "contiguous" to mean "[s]haring an edge or boundary; touching. . . . [c]onnected in . . . space without a break."

The same dictionary defines the term "mesa" as a "broad flat-topped elevation with one or more clifflike sides." Notably, "elevation" means "[a]n elevated place or position."

The term "web" is defined in the American Heritage College Dictionary, Third Edition, as a "latticed or woven structure. . . . [a] complex interconnected structure or arrangement."

From these definitions, it is clear that "contiguous mesas" comprise elevated regions of the recited storage poly (claims 31, 32, and 35), while a storage poly that has a "web-like structure" that comprises a plurality of "contiguous top surfaces" or that comprises "contiguous webs" refers to the interconnectedness of the top surfaces of the storage poly (claims 32, 33, and 40). In view of these plain definitions, it is respectfully submitted that one of ordinary skill in the art would readily understand the terminology used in claims 31-35 and 40 refers to the upper portions of the storage poly, not to the bases thereof.

Further, Fig. 22 of the above-referenced application clearly shows a storage poly structure (the light regions) with both a web-like and maze-like appearance.

In view of these definitions and the clear depictions of this subject matter in the drawings of the above-referenced application, there is no need to limit the scope of any of the claims by identifying which part of the structures shown in Figs. 9 and 22 of the above-referenced application constitute mesas, webs, and the tops, bottoms, beginning points, and ending points thereof.

In view of the foregoing, it is respectfully submitted that there is nothing indefinite about the subject matter recited in claims 31-35 and 40, and it is, therefore, respectfully requested that the 35 U.S.C. § 112, second paragraph, rejections of these claims be withdrawn.

Rejections Under 35 U.S.C. § 102(b)

Claims 31-35 and 37-45 stand rejected under 35 U.S.C. § 102(b).

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Woo

Claims 31-34 stand rejected under 35 U.S.C. § 102(b) for being directed to subject matter which is purportedly anticipated by the subject matter disclosed in U.S. Patent 5,405,799 to Woo et al. (hereinafter "Woo").

Woo describes a structure that, as depicted in FIG. 2 thereof, includes a bottom conductive plate 16, conductive bars 23 thereon, and an upper conductive plate 25 over the bars 23, with the bars 23 electrically connecting the bottom conductive plate 16 and the upper conductive plate 25. At col. 4, lines 9-14, and in FIG. 10, Woo describes and illustrates the bars 23 as comprising a polysilicon layer 18 that "remain[s] as islands of various shapes" which overlie remaining portions of an insulating layer 17, which portions are also referred to in Woo as an insulating layer pattern 19. *See* FIGs. 5 and 6; col. 3, lines 27-38. Thus, the islands of the polysilicon layer 18 of Woo are not connected to one another, or contiguous. Also, the insulating layer 17 of Woo separates the islands of the polysilicon layer 18 from the conductive plate 16 thereof. *See* FIGs. 5 and 6; col. 3, lines 27-38.

Moreover, the polysilicon layer 18 of Woo is not a storage poly—it comprises a mask which is used to form an insulating layer pattern 19. FIG. 6, col. 3, lines 34-38. The insulating

layer pattern 19, in turn, is to be subsequently used to define an upper electrode of a capacitor as a layer 20 of conductive material is deposited over and between the insulating layer pattern 19. FIG. 7; col. 3, lines 39-48.

Independent claim 31 recites a semiconductor storage capacitor poly that includes downwardly extending recesses and a plurality of contiguous mesas that comprise a plurality of contiguous top surfaces forming a maze-like structure.

The storage electrode 30 shown in FIG. 2 of Woo is an entire storage capacitor, including a lower conductive plate 16, a capacitor dielectric, or insulating pattern 19, that includes bars 23, and an upper conductive plate 20 that includes portions which extend downwardly between bars 23. Thus, it is clear that the polysilicon layer 18 of Woo, which acts merely as a mask for forming insulating pattern 19 from a layer 17 of dielectric material, is not a storage poly. FIGs. 4-7; col. 3, lines 10-48. Therefore, Woo lacks any express or inherent description of a storage poly that includes a plurality of mesas but, rather, describes a mask (formed by polysilicon layer 18) and an insulating layer pattern 19 that include a plurality of islands.

Further, the term "islands" refers to structures which are discrete from one another (Merriam-Webster's Collegiate Dictionary, Tenth Edition, defines "island" as "an isolated group or area . . ."). The Tenth Edition of Merriam-Webster's Collegiate Dictionary defines "maze" as "a confusing intricate network . . ." As noted at col. 4, lines 12-14 of Woo, the elements of the polysilicon layer 18, and thus the bars 23, are islands. Additionally, FIG. 10 of Woo depicts passageways completely surrounding each of the islands of the polysilicon layer 18, through which portions of the insulating layer 17 are exposed. In the version of FIG. 10 of Woo included in the Office Action of November 20, 2004, the items that have been designated "A," "B," and "C" would be part of the same island or mesa. Even assuming, *arguendo*, that A, B, and C were considered to be separate mesas, they do not form anything that resembles "a maze-like" structure, as required by independent claim 31.

Accordingly, it is clear from the description of Woo that the islands of the polysilicon layer 18 do not form a confusing intricate network and, thus, are not themselves maze-like. Thus, the islands or bars 23 that are formed from the dielectric layer 17 by using the polysilicon layer 18 as a mask would not be maze-like either.

Further, the term "contiguous" is defined by Merriam-Webster's Collegiate Dictionary, Tenth Edition, as "being in actual contact; touching along a boundary or at a point . . . touching or connected throughout in an unbroken sequence . . ." As used in independent claim 31, it is clear that the mesas themselves must be connected to one another, and that the top surfaces of the mesas must be connected to one another. In contrast, the insulating layer pattern 19 of Woo, which is formed from dielectric layer 17 and has assumed the disconnected island configuration of the overlying mask (polysilicon layer 18), comprises a plurality of disconnected islands or bars 23. While these islands or bars 23 border the material of the upper conductive plate 20, they do not share a border with each other. Moreover, despite the fact that the lower conductive plate 16 serves as a common base or support for the islands or bars of the insulating layer pattern 19, the lower conductive plate 16 does not in any way cause the islands or bars 23 to contact, border, or otherwise become contiguous with one another.

Moreover, as the islands or bars 23 of the insulating layer pattern 19 of Woo are formed prior to deposition of conductive material therearound, the resulting upper conductive plate 20, if it could be properly referred to as a "storage poly," does not include downwardly extending recesses, as recited in independent claim 31.

For these reasons, it is respectfully submitted that Woo does not anticipate each and every element of independent claim 31 and that, under 35 U.S.C. § 102(b), independent claim 31 recites subject matter which is allowable over that described in Woo.

Claim 32 is allowable, among other reasons, as depending from claim 31, which is allowable.

Independent claim 33 also recites a semiconductor capacitor storage poly. The capacitor storage poly of independent claim 33 includes downwardly extending recesses, a plurality of contiguous webs that comprise contiguous top surfaces, and HSG polysilicon on at least some of the contiguous top surfaces.

Again, the polysilicon layer 18 of Woo is not a storage poly—it is a mask which is used to form an insulating layer pattern 19 that is to be subsequently used to define a storage poly (conductive layer 20).

Furthermore, Woo includes no express or inherent description of a storage poly structure that includes downwardly extending recesses. Rather, the conductive layer 20 if Woo, which is the only feature described therein that could be reasonably referred to as a "storage poly," is formed over the islands or bars 23 of an insulating layer pattern 19 have already been formed. Thus, the structures that are described in Woo could not include any recesses that extend downwardly into the conductive layer 20 but, rather, recesses that extend upwardly into the conductive layer 20 and that are instantaneously filled with the islands or bars 23.

Moreover, Woo lacks any express or inherent description of a capacitor storage poly that includes a plurality of contiguous webs that comprise a plurality of contiguous top surfaces. Instead of contiguous webs, the description of Woo is limited to a polysilicon layer 18 which includes "islands of various shapes." Col. 4, lines 12-14 (emphasis supplied). When the underlying dielectric layer 17 is patterned to form an insulating layer pattern 19, the islands or bars 23 of the insulating layer pattern 19 assume the shapes of the islands of the mask (i.e., the polysilicon layer 18). As the term "islands" refers to structures which are discrete from one another, and since Woo does not describe that the islands of polysilicon layer 18 may be connected to or share a border with one another, it is clear that none of the islands of polysilicon layer 18, the islands or bars 23 of the insulating layer pattern layer 19, or their top surfaces is contiguous with any other island or bar.

Accordingly, it is respectfully submitted that Woo does not anticipate each and every element of independent claim 33. It is, therefore, submitted that, under 35 U.S.C. § 102(b), independent claim 33 recites subject matter which is allowable over that described in Woo.

Claim 34 is allowable, among other reasons, as depending from claim 33, which is allowable.

<u>Jun</u>

Claims 35 and 37-45 stand rejected under 35 U.S.C. § 102(b) for reciting subject matter which is purportedly anticipated by the description of U.S. Patent 5,256,587 to Jun et al. (hereinafter "Jun").

As has been noted in the outstanding Office Action, Jun describes patterned polysilicon structures that include upwardly protruding "fingers." *See* FIGs. 4a-4d. Portions of hemispherical grain particles 14 may remain on upper ends of the fingers. In addition, an insulation layer 15, which acts as a mask, may be located over the remaining portions of the hemispherical grain particles 14 that remain on the upper ends of the fingers.

Independent claim Independent claim 35 recites an intermediate semiconductor capacitor structure that includes a storage poly structure, a contiguous HSG polysilicon layer on and in contact with the storage poly structure, and a mask over the HSG polysilicon layer. Recesses in the storage poly structure are exposed through the contiguous HSG polysilicon layer and the mask.

Independent claim 37 recites an intermediate semiconductor memory cell structure that includes a storage poly structure, a plurality of contiguous low elevation regions of an HSG polysilicon layer on and in contact with the storage poly structure, recesses formed in the storage poly structure laterally between the low elevation regions, and dielectric material at least lining the recesses.

The portions of the structures shown in Jun that would be analogous to the "low elevation regions of [the] HSG polysilicon layer" recited in independent claim 37 are the remaining portions of the hemispherical grain particles 14 shown in FIGs. 4c and 4d of Jun. Jun does not expressly or inherently describe that the remaining portions of the hemispherical grain particles 14 are contiguous with one another. Rather, in FIGs. 4c and 4d of Jun, the remaining portions of the hemispherical grain particles 14 appear to be quite separated from each other.

It is, therefore, respectfully submitted that Jun does not anticipate each and every element of independent claim 37. As such, it is respectfully submitted that independent claim 37 recites subject matter which is allowable over that described in Jun.

Independent claim 38, as amended and presented herein, recites a semiconductor memory cell structure that includes "regions of hemispherical-grain polysilicon on at least portions of an upper surface of said storage poly structure . . . and a dielectric layer substantially coating an

upper surface of said storage poly structure and substantially lining each of [a] plurality of recesses." The plurality of recesses impart the storage poly structure with a structure that resembles a plurality of contiguous mesas.

Jun neither expressly nor inherently describes that the polysilicon fingers describe therein resemble "a plurality of contiguous mesas," as is required by amended independent claim 38.

Therefore, Jun does not anticipate each and every element of amended independent claim 38, as would be required to maintain the 35 U.S.C. § 102(b) rejection thereof.

Accordingly, it is respectfully submitted that, under 35 U.S.C. § 102(b), amended independent claim 38 is directed to subject matter which is allowable over the disclosure of Jun.

Each of claims 39-41 is allowable, among other reasons, for depending either directly or indirectly from claim 38.

Claim 40 is further allowable since Jun lacks any express or inherent description of a semiconductor memory cell structure that includes HSG having a web-like appearance. Instead, the description of Jun is limited to isolated remainders of hemispherical grain particles 14.

Independent claim 42, as amended and presented herein, recites an intermediate semiconductor capacitor structure that includes a storage poly structure, a substantially confluent HSG polysilicon layer on the storage poly structure, and a mask positioned over the HSG polysilicon layer. Planarized portions of the HSG polysilicon layer are exposed through the mask.

The description of Jun is limited to processes in which upper elevation portions of the hemispherical grain particles 14 disclosed therein protrude from the dielectric layer 16. Jun does not expressly or inherently describe a structure which includes planarized portions of a hemispherical-grain polysilicon layer that are exposed through a mask, as recited in amended independent claim 42.

Therefore, Jun does not anticipate each and every element of amended independent claim 42. It is, therefore, respectfully submitted that, under 35 U.S.C. § 102(b), amended independent claim 42 is drawn to subject matter which is allowable over the subject matter described in Jun.

Independent claim 43, as amended and presented herein, also recites an intermediate semiconductor capacitor structure. The intermediate semiconductor capacitor structure of independent claim 43 includes a storage poly structure with recesses therein, remaining portions of an HSG polysilicon layer substantially overlying upper portions of the storage poly structure, and a mask positioned over the HSG polysilicon layer. The HSG polysilicon layer has a web-like appearance. The mask is located laterally between the recesses in the storage poly structure, with the recesses being exposed therethrough, and is substantially spaced apart from the storage poly structure by way of the remaining portions of HSG polysilicon layer.

Independent claim 44, as amended and presented herein, recites an intermediate semiconductor capacitor structure that includes a storage poly structure with recesses therein, an HSG polysilicon layer having a web-like appearance on at least portions of the storage poly structure, and dielectric material lining at least the recesses.

Independent claim 45, as amended and presented herein, is directed to an intermediate semiconductor memory cell structure that includes a storage poly with recesses therein, low elevation regions of an HSG polysilicon layer substantially covering an upper surface of the storage poly structure, and dielectric material at least lining the recesses. The HSG polysilicon layer of amended independent claim 45 has a web-like appearance.

As noted previously herein, the description of Jun is limited to remainders of hemispherical grain particles 14 that are isolated from one another. Jun does not expressly or inherently describe that the hemispherical grain particles 14 disclosed therein have a collective web-like appearance, as recited in each of amended independent claims 43, 44, and 45.

Therefore, Jun does not anticipate each and every element of any of amended independent claims 43, 44, or 45, as would be required to maintain the 35 U.S.C. § 102(b) rejections of these claims.

In view of the foregoing, it is respectfully requested that the 35 U.S.C. § 102(b) rejections of claims 31-35 and 37-45 be withdrawn.



CONCLUSION

It is respectfully submitted that each of claims 31-35 and 37-45 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully submitted,

Brick G. Power

Registration No. 38,581

Attorney for Applicants

TRASKBRITT, PC

P.O. Box 2550

Salt Lake City, Utah 84110-2550

Telephone: 801-532-1922

Date: February 19, 2004

BGP/nj:dp
Document in ProLaw

RECEIVED

FEB 2 7 2004